

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Jung Pill Kim

Serial No.: 10/716,749

Confirmation No.: 6180

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Filed: November 19, 2003

Group Art Unit: 2827

Examiner: Trong Q. Phan

For: INTERNAL VOLTAGE GENERATOR WITH TEMPERATURE CONTROL

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office to fax number 571-273-8300 to the attention of Examiner Steve N. Nguyen, or electronically transmitted via EFS-Web, on the date shown below:

January 9, 2007
Date

A. M. Magness
David M. Magness

REMARKS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

In conjunction with the Notice of Appeal filed herewith, Applicant requests a Panel review of the Final Rejection in this matter. Although the remarks herein are focused on specific issues raised by the rejection, nothing in this paper is meant to limit the scope of any arguments, either factual or legal, that Applicant may later present in a full appeal brief.

QUESTIONS FOR REVIEW

Applicant respectfully submits that review is appropriate because the Examiner has failed to properly establish that the cited reference teaches all the claim limitations of the present claims as required under 35 U.S.C. 102(e). Also, as described below, Applicant respectfully submits that the Examiner's rejection of the pending claims under nonstatutory obviousness-type double patenting is incorrect because it does not apply the correct legal test for nonstatutory obviousness-type double patenting.

REMARKS

Claim Rejections - 35 U.S.C. § 102

Claims 1, 3, 5-6, 9-14, 16-19, 21, 23 and 25-30 are rejected under 35 U.S.C. 102(e) as being anticipated by *Snyder et al.* (US Pat. No. 6,829,190, hereinafter *Snyder*). Applicant respectfully traverses this rejection.

First, with respect to claims 12, 21, 22, 23, and 27, the claims were previously cancelled. Accordingly, withdrawal of the rejection with respect to claims 12, 21, 22, 23, and 27 is respectfully requested. See *Final Office Action dated September 15, 2006*, Page 2, Item 2.

In the present rejection, the Examiner cites *Snyder* in rejecting the pending claims. *Snyder* relates to a method for programming a memory device, which can apply a programming voltage and programming time for a specific memory device and which can utilize the memory device temperature when calculating the programming voltage and programming time for a specific memory device. See Col. 2, Lines 50-59.

As an initial matter, Applicant respectfully submits that the Examiner has not made a proper rejection with respect to each of the pending claims. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Thus, to support a rejection under 35 U.S.C. § 102(e), the prior art reference cited by the Examiner must teach each element of each rejected claim. See *id.* In the current rejection, the Examiner has not mapped each claim element to a teaching in the cited reference, and further submits that the reference, in fact, does not teach each of the claimed elements. See *Final Office Action dated September 15, 2006* (hereinafter *Final Office Action*), Pg. 2, Item 2. With respect to claims 3, 5-6, 9, 11, 13-14, and 16-19, 26, 28, and 29, the Examiner has completely omitted any specific discussion of the language of the claims. For example, with respect to claims 3 and 17, the Examiner has omitted any discussion of a refresh rate. With respect to claims 5 and 13, and dependents therefrom, the Examiner has omitted any discussion of a detector and a

reference. Accordingly, Applicant respectfully submits that the Examiner has not met the burden of showing that each element of each rejected claim is cited in the prior art reference. Therefore, withdrawal of the rejection is respectfully requested.

In the present rejection, the Examiner states that *Snyder* describes a programmable voltage pump that can produce a range of programming voltages to a memory device as a function of temperature and time, citing Column 6, Lines 37-39 and Column 8, Lines 16-18 of *Snyder*. See *Final Office Action*, Pg. 2, Item 2. The Examiner states that the programmable voltage pump produces a boosted voltage VPP pump which is applied to the word lines of a memory device, citing *Snyder* at Column 11, Line 17. See *id.* The Examiner then refers to Figures 5C and 5D of *Snyder*, stating that the figures "inherently illustrate that as the temperature decreases, the programming voltage to the memory device increases".

With respect to the cited Figure 5D, the cited figure does not depict the boosted voltage VPP (or any programming voltage) which the Examiner asserts is applied to the word lines of a memory device. This is clear in Figure 5D, which refers to VMP (and does not refer to VPP). See *Snyder*, Figure 5D. This is also clear in the text of *Snyder* which describes Figure 5D, stating that the graph "shows saturation voltage versus pulse width" (emphasis added). *Snyder*, Column 10, Lines 65-66. Thus, the cited margin voltage VMP is a saturation voltage and refers to an intrinsic property of the die (a saturation voltage) and not a programming voltage which is internally generated. Column 10, Line 65 – Column 11, Line 4.

With respect to the explicit teaching of *Snyder* with respect to Figure 5D, *Snyder* merely states that an "ideal pulse width can be determined based on the erase margin saturation curve for each die". Column 10, Line 65 – Column 11, Line 4. Thus, the graph depicted in Figure 5D is used in determining an ideal pulse width. See *id.* Accordingly, the cited figure does not describe selecting a programming voltage as asserted by the Examiner. See *id.* Withdrawal of the rejection is respectfully requested.

Claim Rejections - 35 U.S.C. § 103

Claims 5-6 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Snyder*, in view of Applicant's Fig. 1 Prior Art. Also, Claims 7-8 and 20 are rejected

under 35 U.S.C. 103(a) as being unpatentable over *Snyder*, in view of Applicant's Fig.1 Prior Art and further in view of *Park et al.*, 6,958,947. In each of the present rejections under 35 U.S.C. 103(a), the Examiner relies on the rejection of the independent claims under 35 U.S.C. Sec. 102 in view of *Snyder*. Applicant respectfully submits that the rejection of the independent claims under 35 U.S.C. Sec. 102 in view of *Snyder* has been overcome as described above. Accordingly, the present rejection under 35 U.S.C. Sec. 103(a) is also believed to be overcome. Therefore, withdrawal of the rejection is respectfully requested.

Claim Rejections - Double Patenting

Claims 1, 3, 5-11, 13-20, 25-26 and 28-30 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-28 of U.S. Patent No. 7,009,904.

In the present rejection, the Examiner states that claims 1-24 of the pending application are not patentably distinct from the claims of U.S. Patent No. 7,009,904 because "the voltage generator as recited in claims 1-24 of the present invention is obviously the same as the voltage generator recited in claims 1-28 of U.S. Patent No. 7,009,904, since they are both drawn to the embodiments as shown in the same Figs. 2-3 and 4A-B in the present invention and in U.S. Patent No. 7,009,904". See *Final Office Action*, Pg. 7, Item 9 (emphasis added). Accordingly, the Examiner appears to argue that the claims of the pending application are not distinct from the claims of U.S. Patent No. 7,009,904 because the drawings of both applications appear similar.

Applicant respectfully submits that the Examiner's rejection of the pending claims under nonstatutory obviousness-type double patenting is incorrect because it does not apply the correct legal test for nonstatutory obviousness-type double patenting. As stated in MPEP § 804(II)(B)(1), "In determining whether a nonstatutory basis exists for a double patenting rejection, the first question to be asked is - does any claim in the application define an invention that is merely an obvious variation of an invention claimed in the patent?". Thus, a nonstatutory obviousness-type double patenting rejection requires examination of the claims in both cases, and not the drawings as

asserted by the Examiner. This is clear from the statement in MPEP § 804(II)(B)(1) that:

Any obviousness-type double patenting rejection should make clear:

(A) The differences between the inventions defined by the conflicting claims - a claim in the patent compared to a claim in the application; and

(B) The reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim at issue would have been an obvious variation of the invention defined in a claim in the patent. (Emphasis Added)

Because the Examiner has not provided any specific comparison of the claims on a claim-by-claim basis and element-by-element basis, Applicant submits that the Examiner has not established the requirements of a nonstatutory obviousness-type double patenting rejection. Withdrawal of the rejection is therefore respectfully requested.

Conclusion

Applicant believes that the foregoing discussion demonstrates the patentability of the present claims over the cited references. Accordingly, Applicant requests that the Panel vacate the rejections and remand the matter to the Examiner with instructions to allow the present claims.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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